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EXAMINER

KERVEROS, JAMES C

ART UNIT

PAPER NUMBER

2133

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/800,841

Applicant(s)

KAPUR ET AL.

Examiner

JAMES C KERVEROS

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-29 are pending and are hereby presented for examination, in response to the AMENDMENT filed 6/1/2004 in reply the Office Action mailed on March 2, 2004.
2. The objection to the abstract of the disclosure is hereby withdrawn in view of a new Abstract provided by the Applicant.
3. Claims rejection under 35 U.S.C. 112, second paragraph, is hereby withdrawn in view of Applicant's amendment to the claims, which recite the proper limitation.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The specification fails to describe the new limitation "wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains", as amended in the independent claims 1, 8, 15 and 22. The specification fails to clearly specify the number of the scan chains, so as

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to enable a person skilled in the art to calculate a range for the scan chains "of greater than one and less than a maximum number".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-8, 11-15, 18-23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Motika et al. (US 5983380).

In view of the Claims 1-29 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement of the new limitation, "wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains", as amended in the independent claims 1, 8, 15 and 22, for examination purpose, the Examiner interprets the number of scan chains range to be greater than one and less than any arbitrary maximum number of scan chains (128-136) Figure 2, as disclosed by Motika.

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Regarding independent Claims 1, 8, 15 and 22, Motika discloses an apparatus and method for a semiconductor integrated circuit device under test (DUT) 14 having a test scan arrangement, for communicating with a tester having a pin capacity through the shift register inputs (SRIs), which load patterns into the chip's shift register latches (SRLs) generated by the tester externally to the DUT 14, Figures 1 and 2, comprising:

Scan chains (128, 130, 132, 134, 136) and reconfiguration logic comprising a plurality of multiplexer (4:1 MUX 146) and a (2:1 MUX) coupled to the scan chains, where the logic selectively changes pin configuration required to test the DUT by reconfiguring the individual length and the number of scan chains based on the "mode select" signal from register 142 and "global weight set select" signal from register 138, where the logic provides the compatibility between the test patterns vectors generated by the tester and the tester external to the DUT, where the first tester has a first pin capacity, when the "mode select" signal at logic level "0" allows the LSSD normal pin configuration and wherein the second tester has a second pin capacity, when the "mode select" signal at logic level "1" allows the WRPLBIST test mode pin configuration, FIGS. 2-4.

Regarding independent Claims 8, 15 and 22, in addition to the common limitations applied to claim 1 above, Motika further discloses a storage medium (array 152) which is loaded with the desired test vector set from the tester developed for a first tester having a first pin capacity.

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Selecting modes using "mode select" at logic level "0" for selecting the LSSD normal pin configuration and "mode select" at logic level "1" for selecting the WRPLBIST test mode pin configuration, FIGS. 2-4.

A device under test DUT 14 for coupling with the first tester having a first pin capacity for receiving test vectors through the shift register inputs (SRI), FIG. 2.

Regarding Claim 4, 11, 18 and 26, Motika discloses reconfiguration logic comprising a plurality of multiplexer (4:1 MUX 146) and a (2:1 MUX) coupled to the scan chains between the selected chains (128, 130, 132, 134, 136) and the selected scan-in pins (SRIs) inputs to the DUT 14, FIG. 2.

Regarding Claim 5, 12, 19 and 27, Motika discloses reconfiguration logic comprising a functional input shift register (Linear Feedback Shift Register (LFSR) 12 for receiving SRI data or test vector 140 and for applying test vectors to integrated circuit device under test (DUT) 14 corresponding to the second tester having a second pin capacity, and a functional output shift register such as multiple input signature register (MISR) 16 for providing output values corresponding to the second pin capacity.

Regarding Claim 6, 13, 20 and 28, Motika discloses reconfiguration logic, which also comprises a respective multiplexer (4:1 MUX 146), for each memory cell of the functional input shift register (12) for selecting between a respective memory cell and a respective functional input pin (SRI) based on the mode signal "global weight set select" signal from register 138, FIGS. 2-4.

Regarding Claim 7, 14, 21 and 29, Motika discloses a protocol unit (register 138) coupled to the mode signal "global weight set select" and further comprising a first test

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sequence "0" binary [00] used for the first tester having a first pin capacity, which allows the normal LSSD normal pin configuration and furthermore comprising a second test sequence "1" binary [01] used for the second tester having a second pin capacity, which allows the WRPLBIST test mode pin configuration, FIGS. 2-4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2, 3, 9, 10, 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. (US 5983380) in view of Omura et al. (US 6311300).

Regarding Claims 2, 3, 9, 10, 16, 17, 24 and 25, Motika does not explicitly disclose that a second pin capacity is less than a first pin capacity and wherein the second pin capacity is approximately more than 64 pins and the first pin capacity is proximately more than 1000 pins. Omura et al. (US 6311300) discloses a semiconductor testing apparatus (50) for testing semiconductor device IC 70 having multiple pins including pin electronics 61 which interfaces with the DUT through contact terminal 71. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to test the multiple pin semiconductor device under

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test, as taught by Omura, in the automatic test equipment of Motika, since Motika provides a pin electronics unit which is flexible for interfacing between an ATE tester and a DUT having different pin capacity, thus avoiding the use of multiple testers.

Response to Arguments

7. Applicant's arguments filed 6/1/2004 have been fully considered but they are not persuasive. Claims 1, 4-8, 11-15, 18-23 and 26-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Motika et al. (US 5983380), and Claims 2, 3, 9, 10, 16, 17, 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. (US 5983380) in view of Omura et al. (US 6311300), as set forth in the Office Action.

Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph, in view of new grounds of rejection, as failing to comply with the written description requirement, because of new matter added in the claims, which is not described in the specification.

8. The Applicant argues that Motika fails to disclose or suggest the new limitation "wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains", in claims 1, 8, 15, and 22, as amended. In response to Applicant's argument, as stated above, independent Claims 1, 8, 15, and 22, are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement because the above new limitation is not described in the specification, in such away so as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention.

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Furthermore, the Examiner interprets the number of scan chains range to be greater than one and less than any arbitrary maximum number of scan chains (128-136) Figure 2, as disclosed by Motika.

9. In response to applicant's argument that there is no suggestion to combine the references, of Motika and Omura, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, Omura et al. (US 6311300) discloses a semiconductor testing apparatus (50) for testing semiconductor device IC 70 having multiple pins including pin electronics 61 which interfaces with the DUT through contact terminal 71. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to test the multiple pin semiconductor device under test, as taught by Omura, in the automatic test equipment of Motika, since Motika provides a pin electronics unit which is flexible for interfacing between an ATE tester and a DUT having different pin capacity, thus avoiding the use of multiple testers.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

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§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
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Date: 29 October 2004
Office Action: Final Rejection

By: 

JAMES C KERVEROS
Examiner
Art Unit 2133


Guy J. LAMARRE
PRIMARY EXAMINER